OIPE JC163
NOV 26 2004
PATENT & TRADEMARK OFFICE

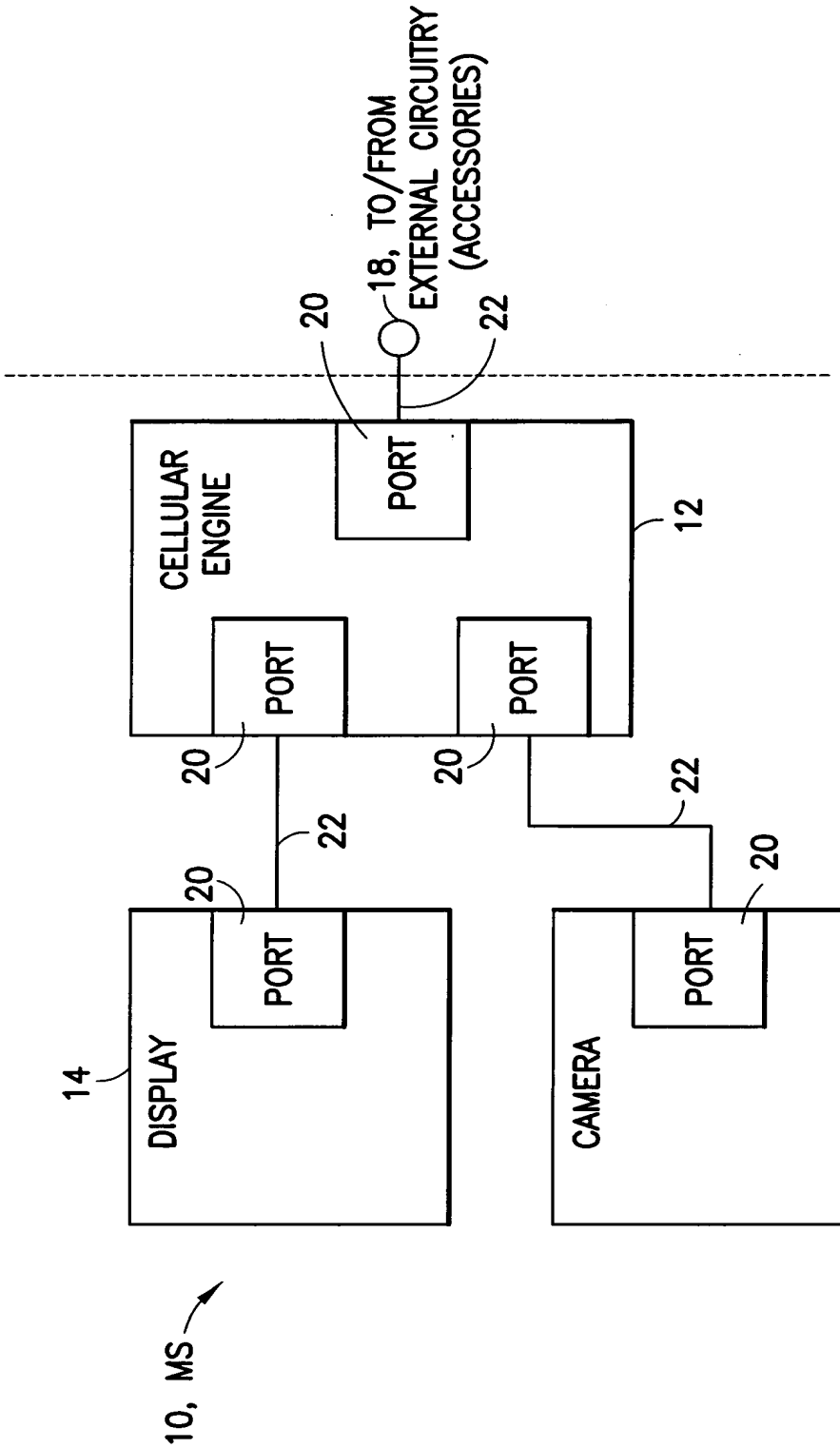


FIG.1

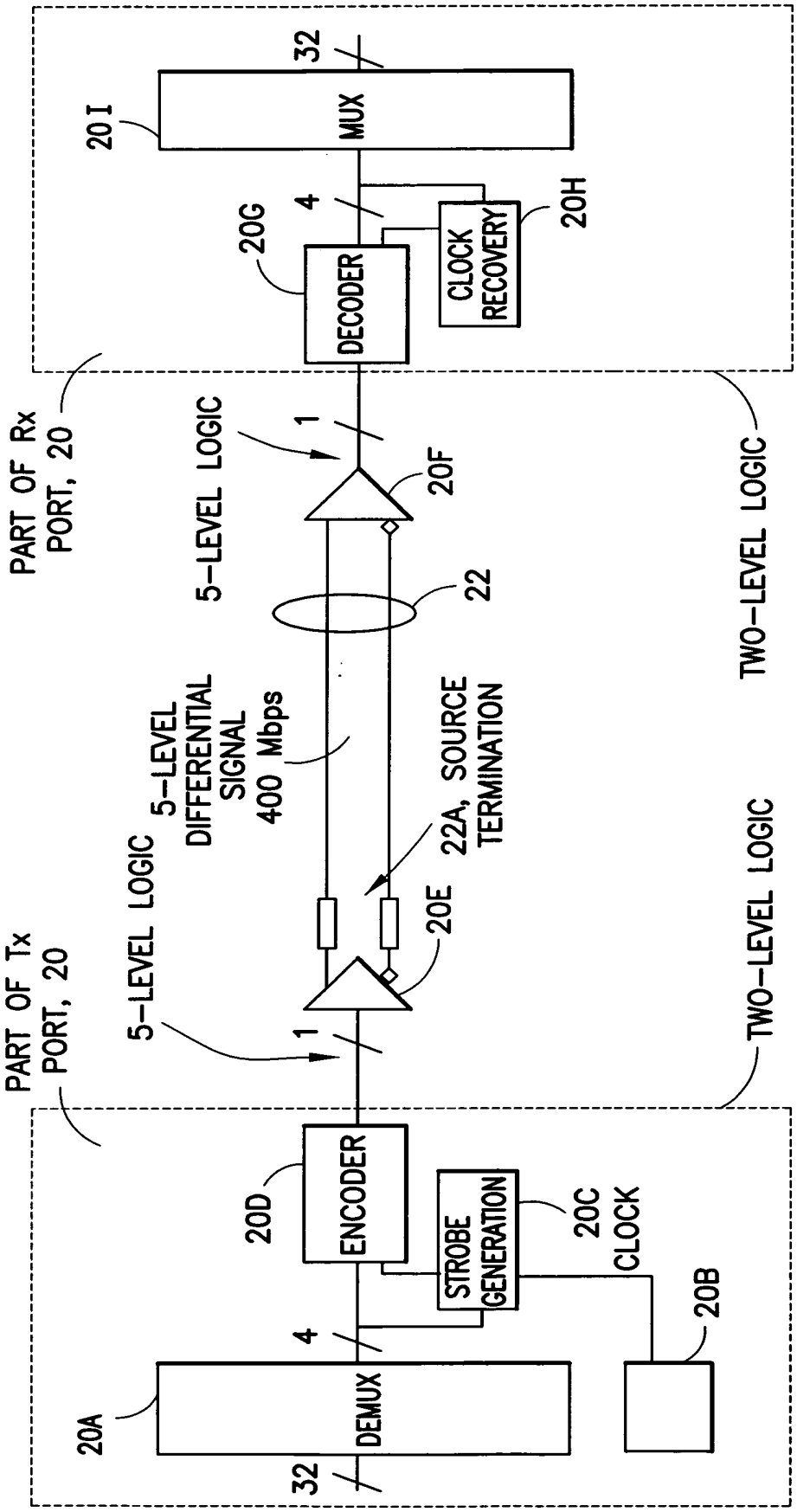

PART OF Tx PORT, 20
PART OF Rx PORT, 20
TWO-LEVEL LOGIC
TWO-LEVEL LOGIC
5-LEVEL LOGIC
5-LEVEL LOGIC
5-LEVEL DIFFERENTIAL SIGNAL 400 Mbps
22A, SOURCE TERMINATION
22
20A
DEMUX
32
4
20B
20C
CLOCK
STROBE GENERATION
20D
ENCODER
1
20E
1
20F
20G
DECODER
4
CLOCK RECOVERY
20H
20 I
MUX
32

FIG.2

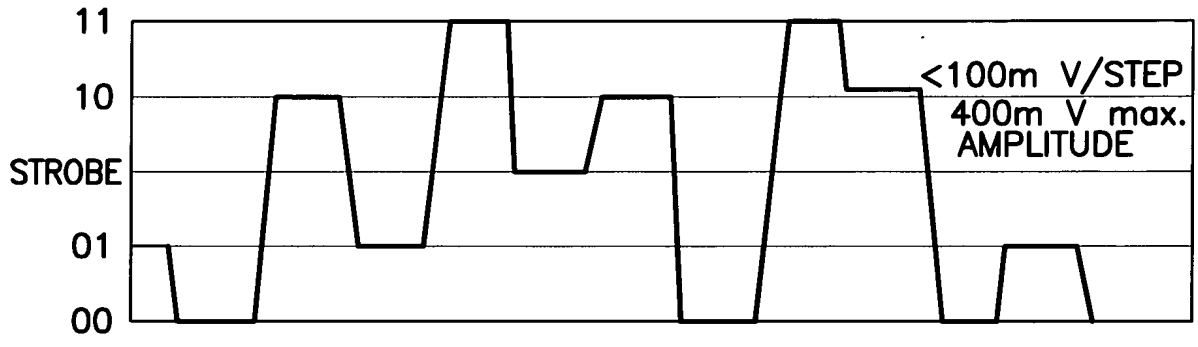


FIG.3A

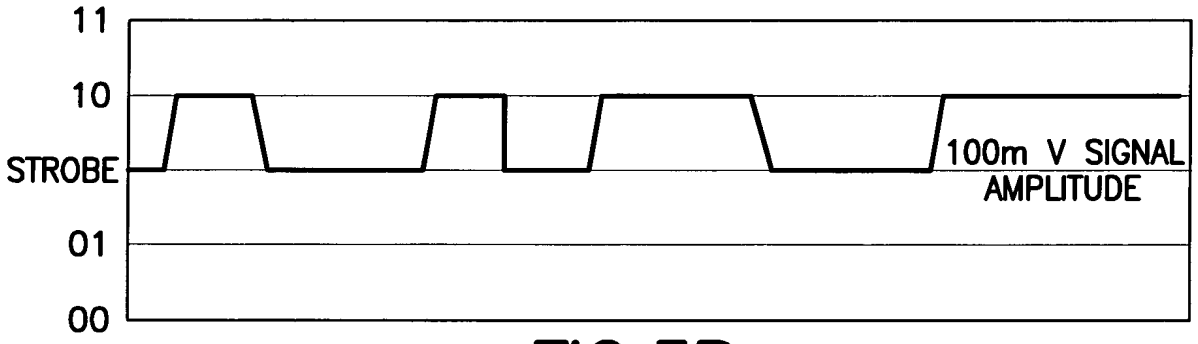


FIG.3B

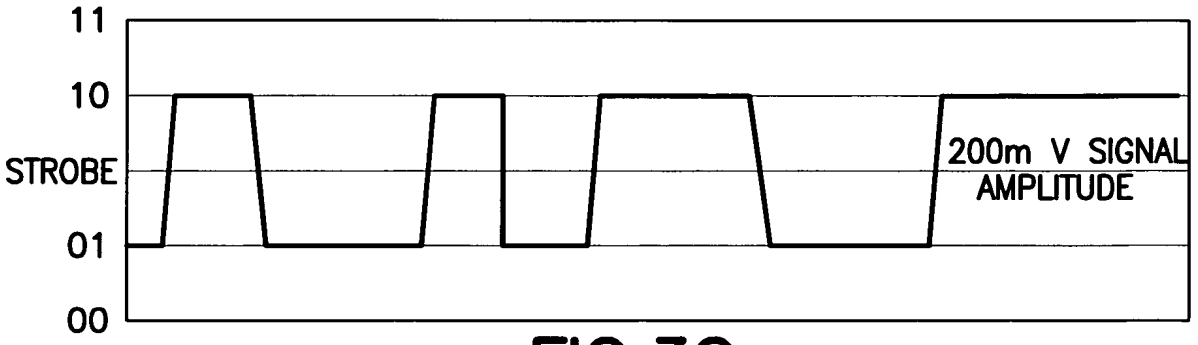
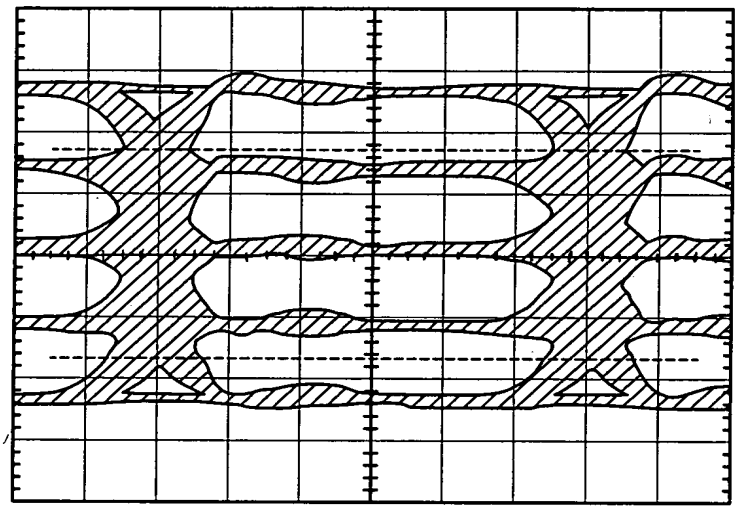
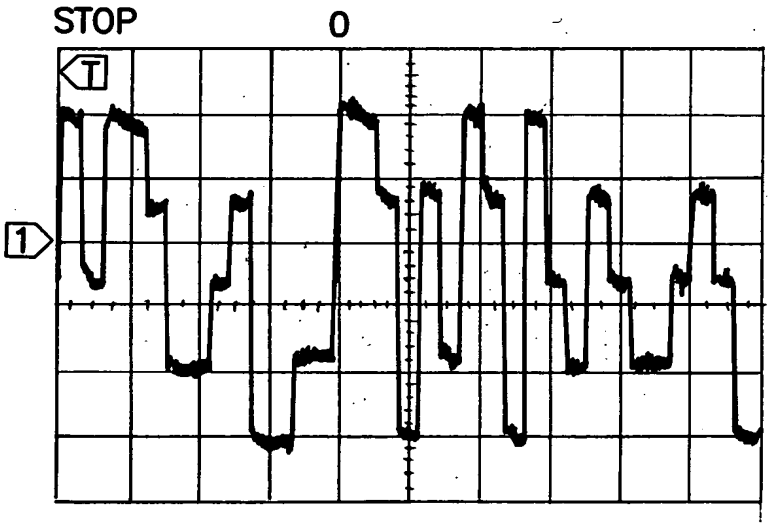


FIG.3C



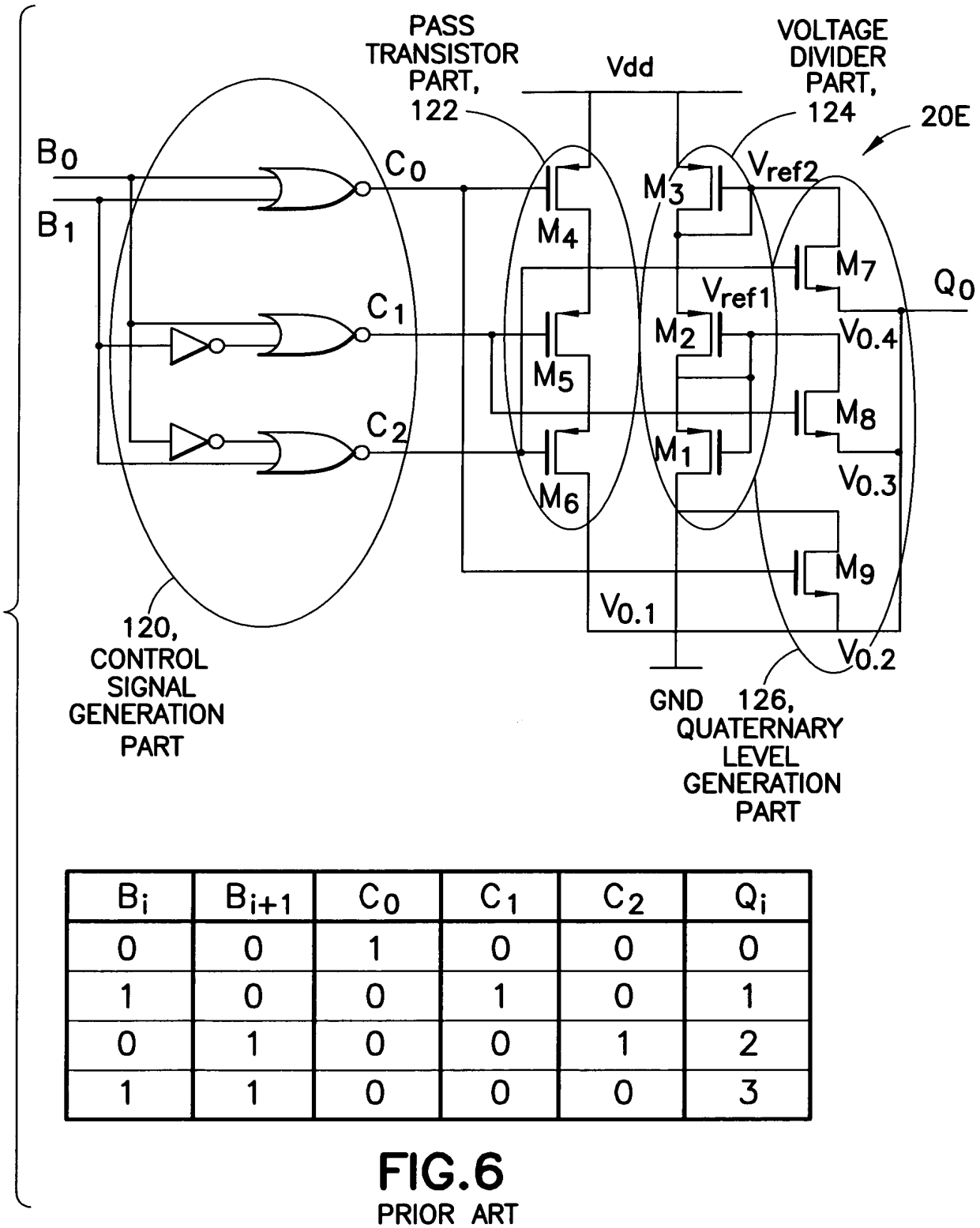
667 MHz
1.5 GBaud

FIG.4
PRIOR ART



30 MHz
60 MBaud

FIG.5
PRIOR ART



B_i	B_{i+1}	C_0	C_1	C_2	Q_i
0	0	1	0	0	0
1	0	0	1	0	1
0	1	0	0	1	2
1	1	0	0	0	3

FIG.6
PRIOR ART

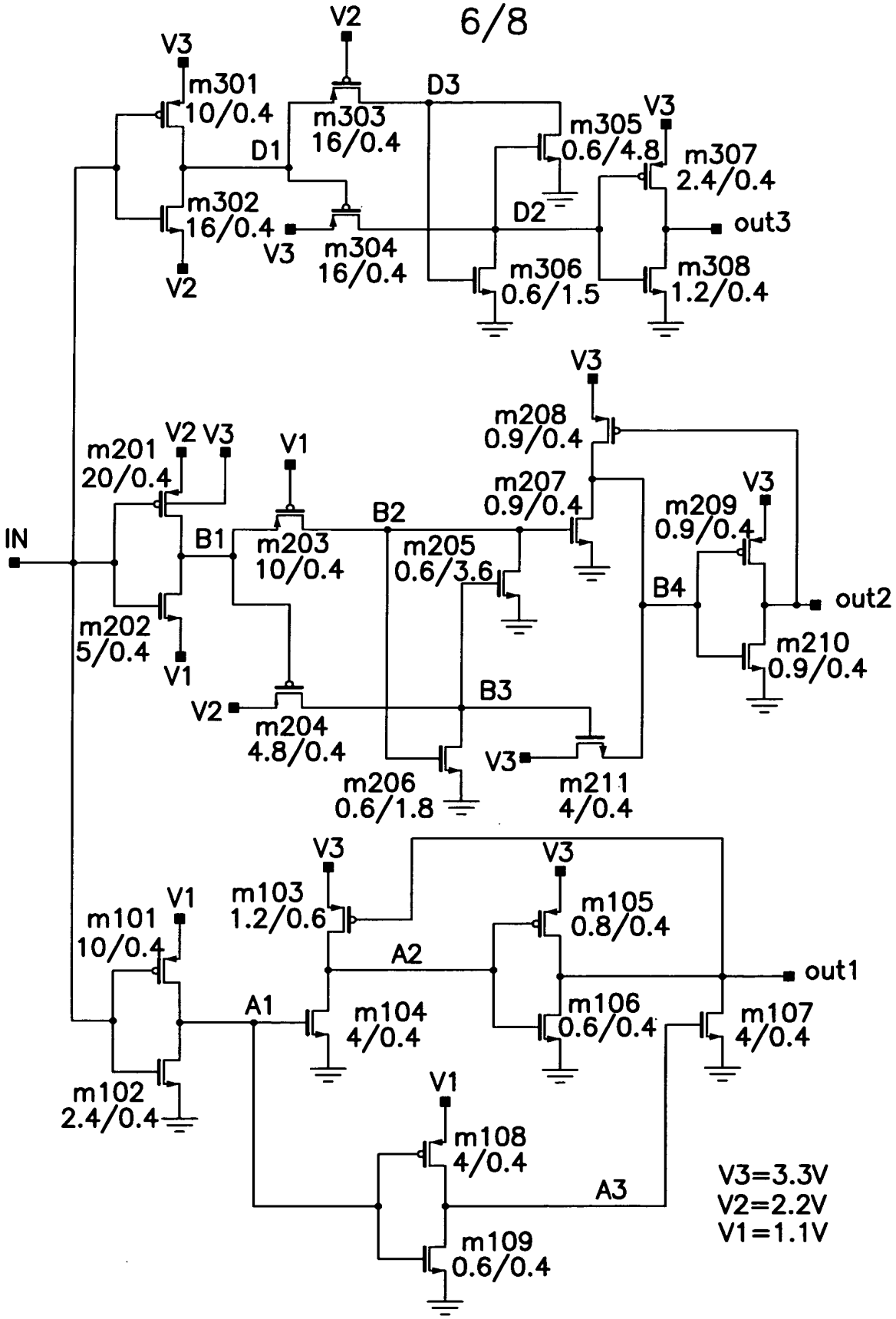


FIG.7
PRIOR ART

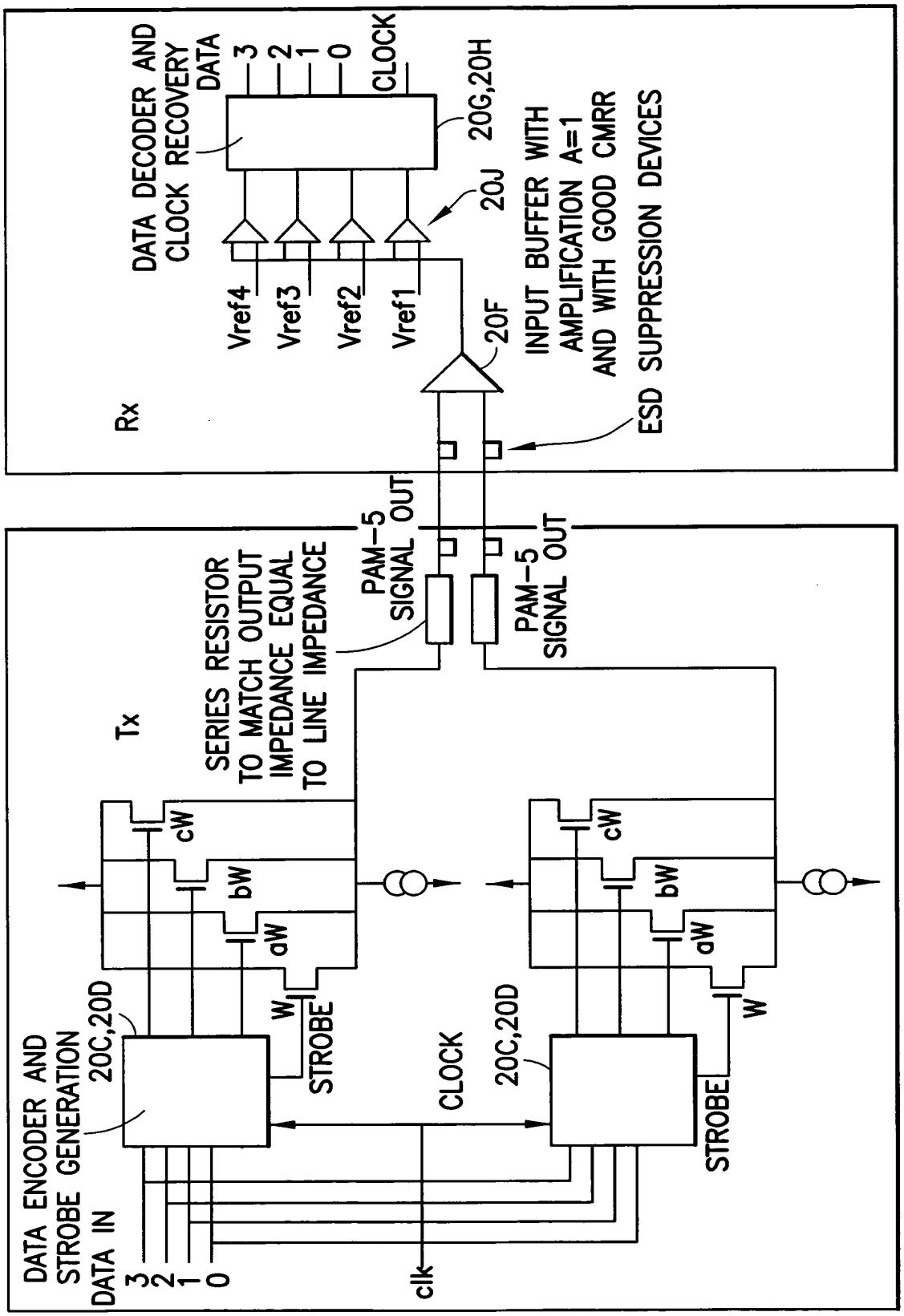

Rx
DATA DECODER AND CLOCK RECOVERY
DATA
3
2
1
0
CLOCK
20G,20H
20J
Vref4
Vref3
Vref2
Vref1
20F
INPUT BUFFER WITH AMPLIFICATION A=1 AND WITH GOOD CMRR
ESD SUPPRESSION DEVICES
Tx
SERIES RESISTOR TO MATCH OUTPUT IMPEDANCE EQUAL TO LINE IMPEDANCE
PAM-5 SIGNAL OUT
PAM-5 SIGNAL OUT
cW
bW
aW
W
STROBE
CLOCK
20C,20D
DATA ENCODER AND STROBE GENERATION
DATA IN
3
2
1
0
clk

FIG.8

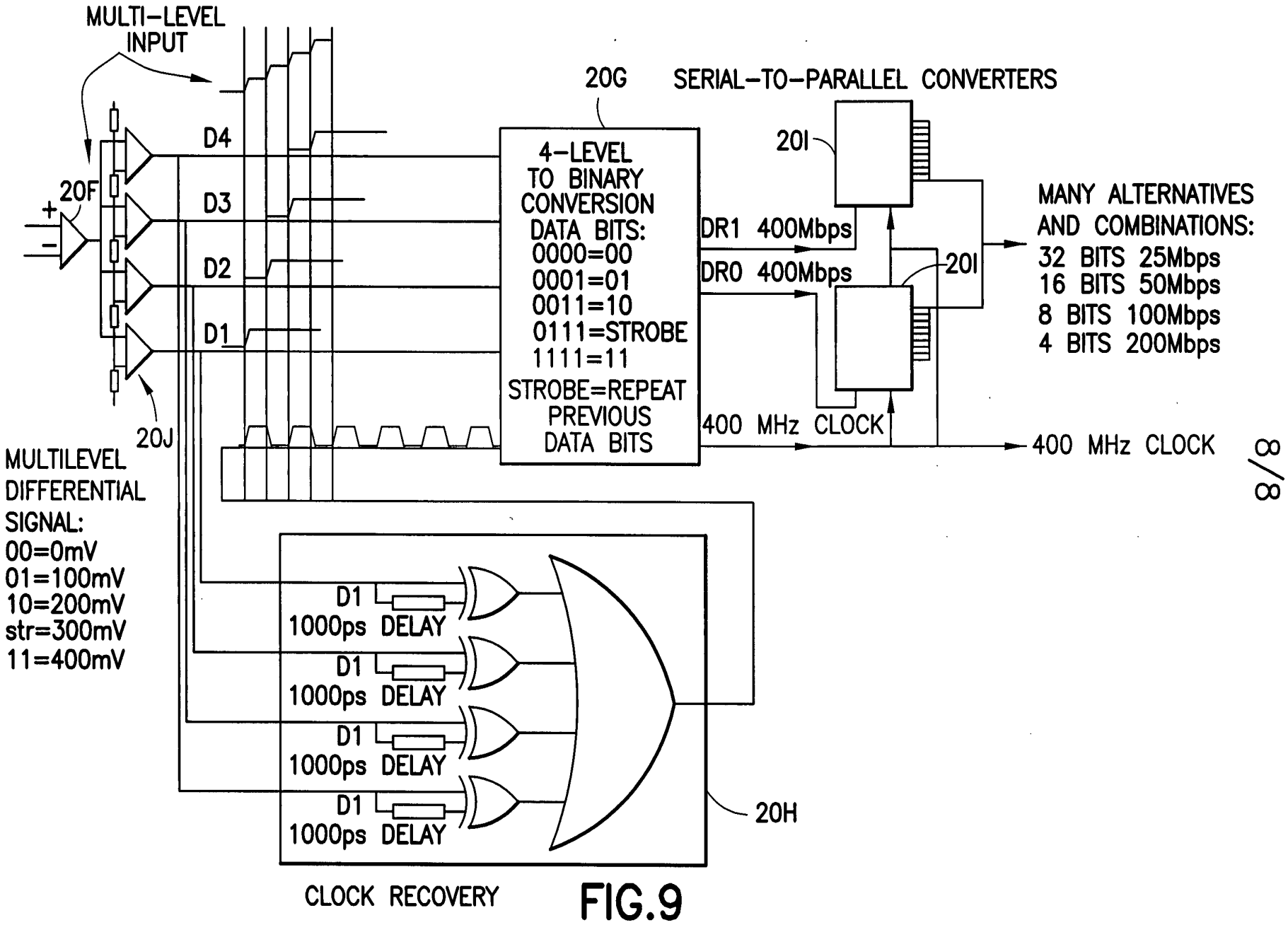

MULTI-LEVEL INPUT
20F
+
-
D4
D3
D2
D1
20J
MULTILEVEL DIFFERENTIAL SIGNAL:
00=0mV
01=100mV
10=200mV
str=300mV
11=400mV
20G
SERIAL-TO-PARALLEL CONVERTERS
4-LEVEL TO BINARY CONVERSION DATA BITS:
0000=00
0001=01
0011=10
0111=STROBE
1111=11
STROBE=REPEAT PREVIOUS DATA BITS
20I
DR1 400Mbps
DR0 400Mbps
400 MHz CLOCK
MANY ALTERNATIVES AND COMBINATIONS:
32 BITS 25Mbps
16 BITS 50Mbps
8 BITS 100Mbps
4 BITS 200Mbps
400 MHz CLOCK
D1
1000ps DELAY
D1
1000ps DELAY
D1
1000ps DELAY
D1
1000ps DELAY
20H
CLOCK RECOVERY

FIG.9